ABSTRACT OF THE DISCLOSURE

A black matrix having an opening at pixels of a matrix array in a display area, a common wire including common pads and common signal lines, and gate pads in a peripheral area, and an alignment key in outer area to align interlayer thin films are formed on an insulating substrate. Red, blue and green color filters the edge of which overlap the black matrix are formed at the pixels on the insulating substrate, and an organic insulating layer covering the black matrix and the color filters and having a contact hole exposing the gate pad is formed thereon. A gate wire including a gate line connected to the gate pad through the contact hole and a gate electrode connected to the gate line is formed on the organic insulating layer, and a gate insulating layer covering the gate wire is formed on the organic insulating layer. A semiconductor pattern and ohmic contact layers are sequentially formed on the gate insulating layer of the gate electrode. A data wire including a source electrode and a drain electrode that are made of a same layer on the ohmic contact layers and separated from each other, and a data line connected to the source electrode and defining the pixels of a matrix array by crossing the gate line is formed on the gate insulating layer. A passivation layer covering the data wire and having contact holes exposing the gate pad and the data pad is formed, and a pixel wire including a pixel electrode, a redundant gate pad, a redundant data pad that are respectively connected to the drain electrode, the gate pad and the data pad through the contact holes.